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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,390	10/31/2003	Yung-Hung Chen	250606-1010	3274

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/699,390	CHEN, YUNG-HUNG	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 11-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 11-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed 06/27/05. The allowable subject matters of claims 10 and 11 in previous office action have been withdrawn. A new ground of rejection is introduced.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4, 6, 8 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Gregorius (US 20030011350) (newly cited).

As to claim 1, Gregorius discloses in figure 1 a voltage reference generator for generating an output voltage (Vout) at an output node, comprising: a level shifter (MN1) for s shifting a first reference voltage (voltage at the gate of MN1) into the output voltage at the output node according to a shift between the first reference voltage and the output voltage; and a feedback circuit (OTA2, MP3, MN4, MN3) for monitoring the output voltage and a second reference voltage (voltage at node between MN2 and MP3) to control the shift and to normalize the output and second reference voltages; and a low-pass filter (Cm1) to filter out a high frequency portion of the first reference voltage and direct the first reference voltage to the level shifter.

As to claim 2, figure 1 shows that the level shifter includes a source follower (MN1) coupled between a voltage source (Vdd) and the output node, the source follower having an input node (gate) for receiving the first reference voltage.

As to claim 3, figure 1 shows that the source follower has an MOS transistor having a drain connected to the voltage source, a source as the output node and a gate at the input node, and further having a current source (MN6) controlled by the feedback circuit and connected to the source of the MOS transistor.

As to claim 4, figure 1 MOS transistor is a NMOS transistor.

As to claim 6, figure 1 shows that the current source is an MOS transistor having a drain connected to the output node, a source connected to a ground, and a gate connected to the output of a differential amplifier (OTA2, MP3, MN4, MN3, MN5).

As to claim 8, figure 1 shows that the MOS transistor is a NMOS transistor.

As to claim 12, figure 1 shows that the feedback circuit has a differential amplifier with an inverted input, a non-inverted input and an output, the non-inverted input coupled to the output node, the inverted input coupled to the second reference voltage, and the output coupled to a current source (MN6) in the level shifter to control the shift of the level.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gregorius (US 20030011350) in view of Khalid (US 20040150464) (previously cited).

Gregorius' figure 1 shows all limitations of the claim except for the MOS transistor is a PMOS transistor. However, Khalid's figures 1A and 1B show that reversing the type of transistors and the polarity in a voltage generation is well known. Therefore, it would have been obvious to one having ordinary skill in the art to reverse the structure of Gregorius' by reversing the transistor types and the power supplies in order to take advantage of the benefit of Gregorius' circuit and use the circuit a different environment that requires a reverse type power supply circuit. Thus, the modified Lim's figure 7 shows the MOS transistor is NMOS transistor.

5. Claims 1-4, 6, 8 and 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (USP 6433521) in view of Shyu et al. (USP 5221890).

As to claim 1, Chen et al.'s 7 discloses in figure 1 a voltage reference generator for generating an output voltage (Vo) at an output node, comprising: a level shifter (14) for s shifting a first reference voltage (voltage at the gate of 14) into the output voltage at the output node according to a shift between the first reference voltage and the output voltage; and a feedback circuit (11) for monitoring the output voltage and a second reference voltage (Vref) to control the shift and to normalize the output and second reference voltages. Thus, figure 7 shows all limitations of the claim except for a low-pass filter coupled to the gate of transistor 14. However, Shyu et al.'s figure 1 shows a circuit having a lowpass filter (12) coupled to the output of amplifier 10 for the purpose of reducing noise. Therefore, it would have been obvious to one having ordinary skill in the art to add lowpass filter to each of the output of Chen et al.'s amplifiers 10 and 11 for the purpose of reducing noises.

As to claim 2, the modified Chen et al.'s figure 7 shows that the level shifter includes a source follower (14) coupled between a voltage source (Vdd) and the output node, the source follower having an input node (gate) for receiving the first reference voltage.

As to claim 3, the modified Chen et al.'s figure 7 shows that the source follower has an MOS transistor having a drain connected to the voltage source, a source as the output node and a gate at the input node, and further having a current source (15) controlled by the feedback circuit and connected to the source of the MOS transistor.

As to claim 4, the modified Chen et al.'s figure 7 shows MOS transistor is a NMOS transistor.

As to claim 6, the modified Chen et al.'s figure 7 shows that the current source is an MOS transistor having a drain connected to the output node, a source connected to a ground, and a gate connected to the output of a differential amplifier (11).

As to claim 8, the modified Chen et al.'s figure 7 shows that the MOS transistor is a NMOS transistor.

As to claim 11, the modified Chen et al.'s figure 7 shows that the low-pass filter comprises at least a capacitor (the newly added filter) connecting an input node of the level shifter and a voltage source.

As to claim 12, the modified Chen et al.'s figure 7 shows that the feedback circuit has a differential amplifier (11) with an inverted input, a non-inverted input and an output, the non-inverted input coupled to the output node, the inverted input coupled to the second reference voltage, and the output coupled to a current source (15) in the level shifter to control the shift of the level.

As to claim 13, the modified Chen et al.'s figure 7 shows that the feedback circuit further has a low-pass filter (the newly added filter) connected between output of the differential amplifier and current source in the level shifter.

As to claim 14, the modified Chen et al.'s figure 7 fails to show a voltage divider to provide the first reference voltage and a third reference voltage. However, it would have been obvious to one having ordinary skill in the art to add a voltage divider coupled to the output of amplifier 10 for the purpose of further providing additional reference voltages.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US 6433521) in view of Shyu et al. (USP 5221890) and Khalid (US 20040150464) (previously cited).

The modified Chen et al.'s figure 7 shows all limitations of the claim except for the MOS transistor is a PMOS transistor. However, Khalid's figures 1A and 1B show that reversing the type of transistors and the polarity in a voltage generation is well known. Therefore, it would have been obvious to one having ordinary skill in the art to reverse the structure of Chen's figure 7 by reversing the transistor types and the power supplies in order to take advantage of the benefit of Chen's circuit and use the circuit a different environment that requires a reverse type power supply circuit. Thus, the modified Chen's figure 7 shows the MOS transistor is NMOS transistor.

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US 6433521) in view of Shyu et al. (USP 5221890) and Shulman (USP 6064258).

The modified Chen et al.'s figure 7 fails to shows a constant current source coupled between the output node and another voltage source. However, Shulman's figure 3 shows a

circuit having plurality of stages connected in parallel in order to reduce offset. Therefore, it would have been obvious to one having ordinary skill in the art to add at least one more stage similar to Chen et al.'s figure 7 and connected in parallel to Chen et al.'s figure 7 for the purpose of reducing offset. Thus, the modified figure 7 further shows a constant current source (the newly added Chen et al.'s 15) coupled between the output node an another voltage source.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUAN TRA
PRIMARY EXAMINER
Art Unit 2816

July 5, 2005